RapidCool™ - A Direct to Chip Liquid Cooling Technology

Enabling the Next-Generation of AI Hardware

Low Thermal Resistance | **Cools High Power Density ICs** | **Application Specific Customization** | **Scalable & Reliable**

Compatible With Advanced Packaging Assembly Supply Chain

Fig. 1: Si Cold Plates Bonded to IC

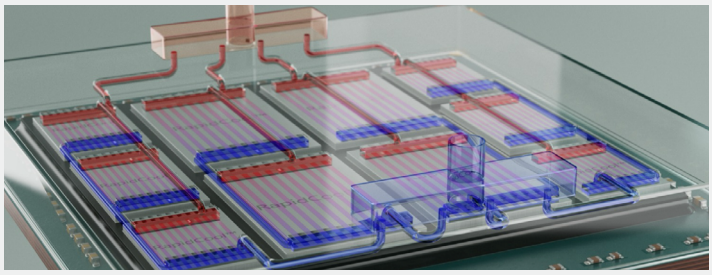

Fig. 2: Integrated Manifold

Key Benefits

- Enables ultra-high power density chipsets (> 5 W/mm^2)
- Reduces junction temperature ($T_{j,max}$) with > 70% thermal resistance reduction over conventional TIM-based cold plates
- Custom thermal design with IC heatmap integration to optimize HPC module performance (cooling both logic and memory)
- Predictive CFD modeling with < 5% variance from experimental results
- Fabricated using standard lithography for custom design, precise channel geometry, and flow control

Technology Overview

Adeia's RapidCool™ is a revolutionary direct-to-chip liquid cooling solution designed for next-generation high-performance systems.

A fully integrated cooling architecture including **silicon cold plates directly bonded** to IC die.

- Advanced **microchannel design** delivers 14% lower thermal resistance over legacy microchannels with 100x lower pressure drop[1]
- **3D-printed manifold** for optimized coolant distribution that seamlessly interfaces with Si cold plate

Industry Applications

- **Data Centers:** Efficient cooling and rapid response to AI/ML power transients
- **High-performance Computing (HPC):** Supports next-generation high-power IC roadmaps

[1] D.B. Tuckerman and R.F.W. Pease, IEEE Electronic Device Letters, EDL-2, No. 5, May 1981.

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Manufacturability, Scalability, & Reliability

Manufacturability & Integration

- Compatible with today's semiconductor packaging supply chain
- Cold plates are fabricated separately in silicon wafers (no IC die etching required)
- Standard processes enable scalable production

Scalability

- Supports multi-die HPC configurations (see Figure 1)
- Modular architecture enables system-level expansion

Reliability

- **No TIM required** → eliminates interface degradation and failure
- **No clamping pressure** → reduces package and board stress
- Bond interface strength exceeds the fracture strength of silicon

Performance Highlights

Fig. 3: Comparisons of Liquid Cooling Methods: Thermal Resistance

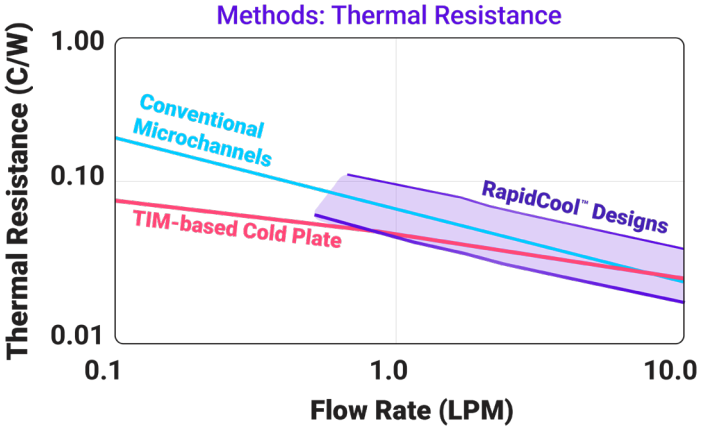

Fig. 4: Comparisons of Liquid Cooling Methods: Pressure Drop

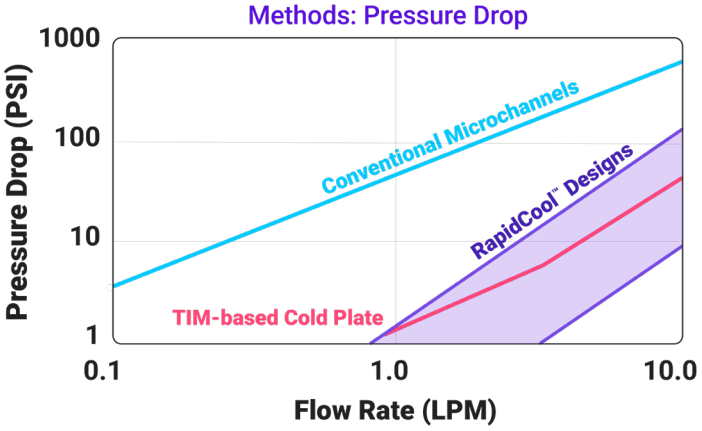

Fig. 5: Pumping Power to Device Power Ratio

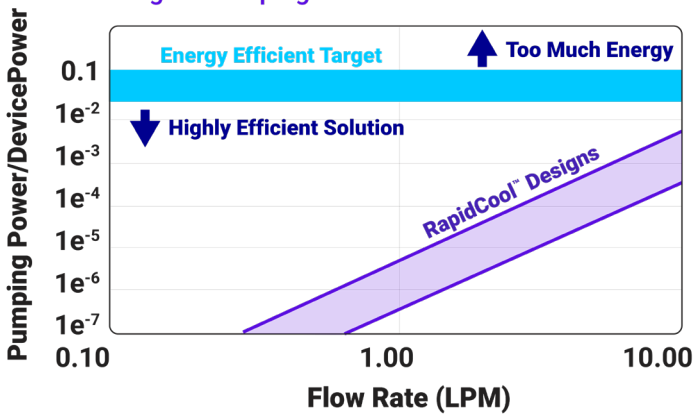

Table 1: Coolable Power Density

Flow Rate (LPM)	Power Density (W/mm2)			
	Design A	Design B	Design C	Design D
0.8	1.2	1.0	0.8	0.8
1.5	1.9	1.4	1.1	1.0
2.3	2.4	1.7	1.4	1.2
3.0	2.9	1.9	1.6	1.4
3.8	3.4	2.2	1.9	1.6
7.6	5.2	3.1	2.8	2.3
11.4	6.4	3.9	3.5	2.9

* 100°C $T_{j,max}$. Uniform power density assumed.

Why Adeia?

Adeia® leads hybrid bonding and advanced packaging with breakthrough interconnect and thermal solutions—powering scalable, high-performance AI and HPC systems.

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