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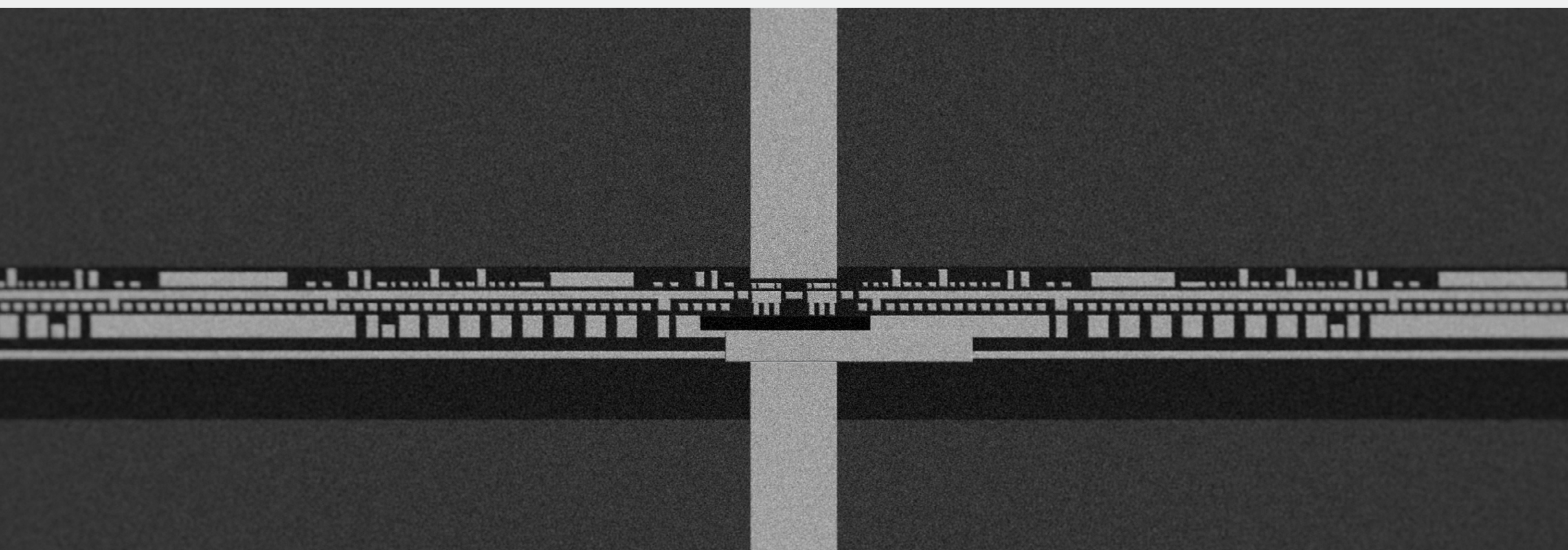
Reworkable Die-to-Wafer Hybrid Bonding Processes Enable Higher-Yield Semiconductor Integration

Introduction

Modern microprocessors are advancing at an extraordinary pace, driven by the demands of high-performance computing (HPC) and artificial intelligence (AI). These applications require unprecedented processing power, massive data bandwidth, high reliability, and efficient thermal management.

Central to this transformation is hybrid bonding, a breakthrough technology that enables far higher interconnect densities than conventional microbump packaging. The result is more compact, highly integrated systems with faster signal transmission and improved overall performance.



Hybrid Bonding: A Closer Look

Hybrid bonding, also known as direct-bond interconnect, is used to stack and join semiconductor components in die-to-die (D2D), die-to-wafer (D2W), and wafer-to-wafer (W2W) configurations.

The process begins with surface preparation. Bonding surfaces are planarized using chemical mechanical planarization (CMP) to achieve extreme flatness, then cleaned and plasma-activated to enable strong, low-temperature initial bonding. The aligned surfaces, positioned with sub-micron precision, are brought into contact, forming an initial bond at room temperature. A subsequent thermal anneal strengthens the interface, creating permanent dielectric bonds and robust copper-to-copper interconnects.

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Advantages of Hybrid Bonding

Hybrid bonding sets a new standard for interconnect density, enabling pitches below 1 μm, far smaller than the 20 – 35 μm limit of traditional microbumps. This fine pitch, combined with the elimination of solder, delivers higher I/O density with lower parasitics (inductance, capacitance, and resistance), and faster, more energy-efficient signal transmission. Thermal performance also improves, as direct metal pathways enhance heat dissipation, an increasingly critical advantage as power densities rise.

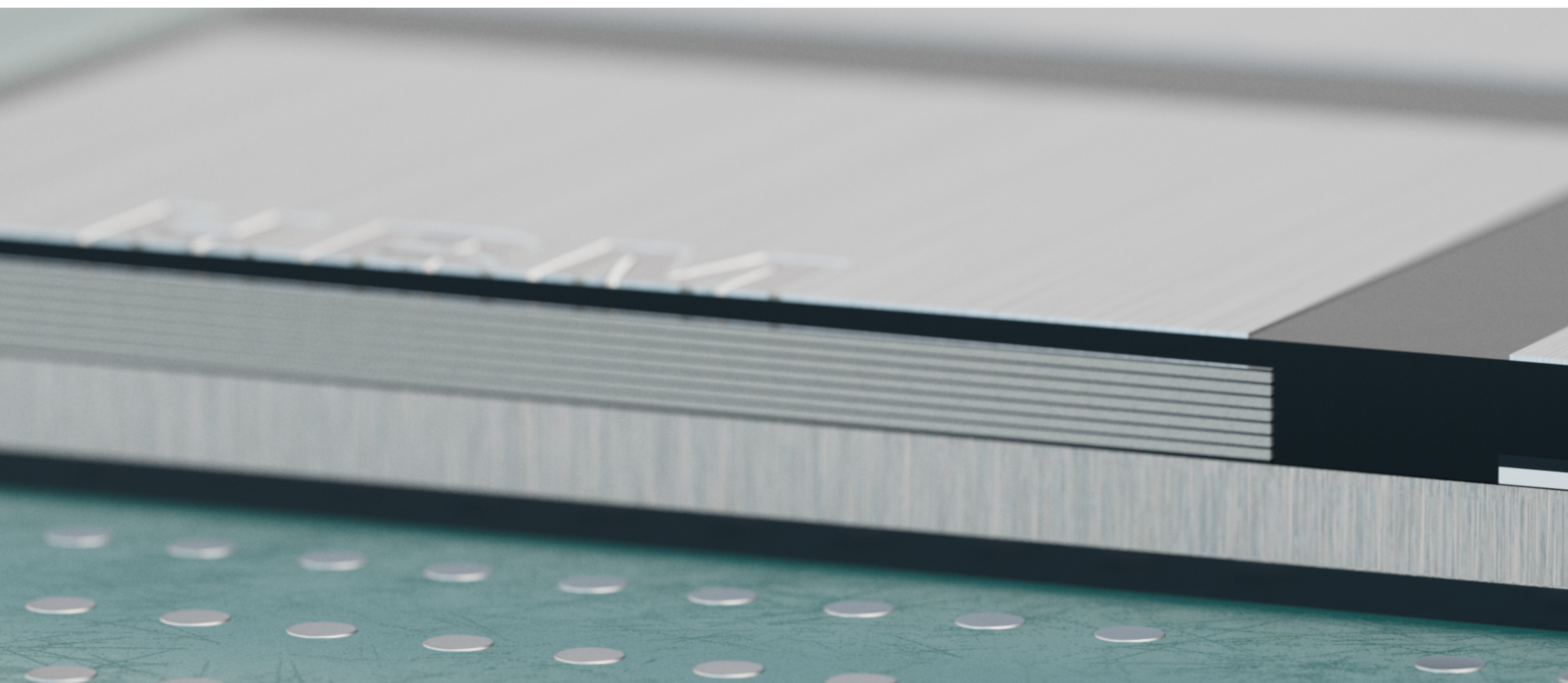
Beyond these performance gains, hybrid bonding enables true three-dimensional (3D) integration. Devices can be stacked without bulky interconnect structures, resulting in more compact systems and higher levels of functional integration. This architecture supports the seamless integration of diverse technologies, such as high-performance logic, high-bandwidth memory (HBM), AI accelerators, chiplets, analog and mixed-signal circuits, RF components, power devices, sensors, and photonics, within a single package, unlocking new possibilities for next-generation semiconductor design.

Manufacturing Challenges

Despite its many advantages, hybrid bonding imposes exceptionally tight manufacturing constraints. The process demands sub-micron alignment accuracy and ultra-clean, defect-free surfaces; even a single microscopic particle contaminant (on the order of a micron) can introduce a void at the bonding interface that disrupts electrical continuity and reduces yield.

With such extreme precision requirements, a key limitation has been the lack of reworkability. Once the die is attached, immediately the dielectric-dielectric bond is quite strong and removal without damaging the bonding surface below seemed impossible. After annealing, it becomes a permanent molecular fusion of dielectric materials and copper-to-copper interconnections that cannot be separated without damaging components. If a defect is discovered, the entire assembly is typically discarded, an outcome that becomes increasingly costly as device complexity and value rise.

This “all-or-nothing” dynamic has emerged as a critical bottleneck to scaling hybrid bonding in high-volume manufacturing. It places intense pressure on upstream process control, inspection, and yield management, highlighting the need for new approaches that enable reworkability without causing damage.



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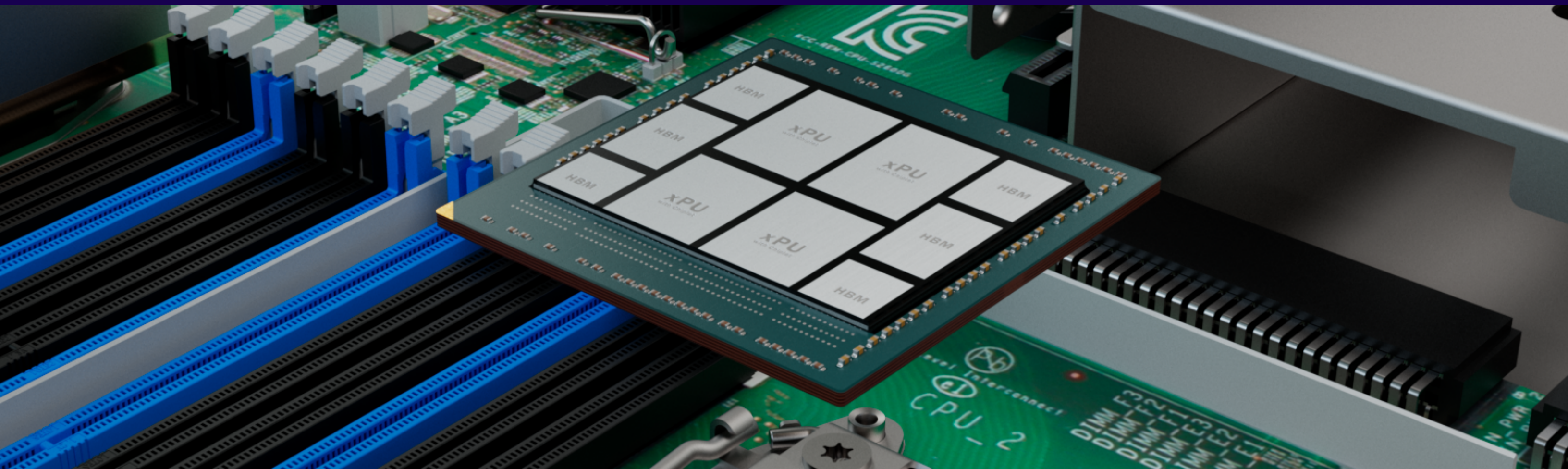

Overcoming the Rework Barrier in Hybrid Bonding

Adeia has introduced reworkable die-to-wafer (D2W) hybrid bonding processes that address one of the technology's most critical limitations. These approaches leverage the fact that immediately after bonding, the bonded interface is relatively weak. It is dominated by the chemical reaction at the interface which increases with time and temperature, creating a window in which defective die can be safely removed and replaced before permanent bonding occurs. This capability fundamentally changes the yield equation for advanced hybrid bonding.

Two complementary die removal techniques have been demonstrated:

- **Blade-based removal** – A custom tool engages a thin blade at the die edge to initiate separation. The die is gently lifted with an upward motion and slight rotation, minimizing stress and avoiding contact with the substrate. A vacuum catcher captures the die immediately upon release.

- **Adhesive-based stud pull removal** - A temporary adhesive attaches a metal stud to the backside of the die, enabling controlled vertical extraction. A precision pull mechanism applies an upward force, minimizing lateral motion and handling damage. Pull force and stud size scale with die thickness and area. For thin dies, the stud spans a large fraction of the die to maintain rigidity and prevent cracking, enabling reliable low-force removal.

Both methods achieve separation by propagating a debond front across the interface and have been successfully demonstrated across a wide range of die sizes and thicknesses, without damaging the die, substrate, or adjacent structures, and without introducing residual particulate contamination.

The rework window extends up to seven days at room temperature and can be further prolonged with cold storage (-20°C), which slows interfacial bond strengthening and extends the window to a month or more. After removal, replacement die can be rebonded using standard processes. Electrical testing of reworked structures shows yields of approximately 95 – 100%, similar to our initial bonding, confirming that rework can be performed without degrading performance or manufacturability.

Looking Ahead

Hybrid bonding continues to evolve, with ongoing innovation focused on finer interconnect pitch, integration with advanced cooling technologies, and automation of rework processes for high-volume manufacturing.

Adeia remains at the forefront of this progress, advancing ultra-fine hybrid bonding through its Direct Bond Interconnect (DBI® Ultra) platform. By enabling sub-micron pitch scaling and supporting 2.5D, 3D, and 3.5D heterogeneous integration, DBI® Ultra is well positioned to drive next-generation of chiplet-based architectures for HPC and AI systems.

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